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12EC020

M.Tech. Degree Examination, June/July 2015
CMOS RF Circuit Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions.***

1 a. Explain the effect of nonlinearity in a typical RF system with respect to gain compression, cross modulation and intermodulation. **(12 Marks)**

b. An amplifier designed to operate at 2GHz with a gain of 10dB has two signals of equal power applied at the input. One is at a frequency of 2GHz and another at a frequency of 2.01GHz. At the output, four tones are observed at 1.99, 2.0, 2.01 and 2.02GHz. The power levels of the tones are -70, -20, -20 and -70 dBm respectively. Determine the $11P_3$ and 1dB compression point for this amplifier. **(08 Marks)**

2 a. Discuss the different types of noise associated with a MOSFET. Give expressions for each type of noise. **(06 Marks)**

b. Calculate the total output noise power of the following circuit. Neglect channel length modulation. [Express the noise power in terms of current]. **(04 Marks)**

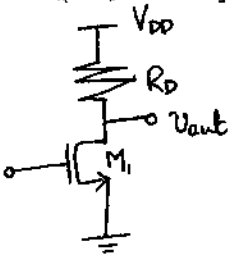

Fig.Q.2(b)

c. Explain sensitivity and dynamic range with respect to a RF receiver. Derive the expression for spurious free dynamic range (SFDR)? **(10 Marks)**

3 a. Compare TDMA, FDMA and CDMA techniques in detail. **(06 Marks)**

b. Explain the architecture of a dual IF heterodyne receiver with a neat block diagram. **(08 Marks)**

c. Discuss the trade off between image rejection and channel selection in a heterodyne receiver. **(06 Marks)**

4 a. Explain the Hastley architecture of image reject receiver. Derive the mathematical relation to show that image rejection is possible. **(12 Marks)**

b. Draw a neat sketch of a direct conversion receiver and list the different issues associated with this receiver. **(08 Marks)**

5 a. Draw the complete small signal equivalent circuit of MOSFET at high frequency. **(05 Marks)**

b. Explain one method used to generate quadrature signals in an RF receiver. **(05 Marks)**

c. Calculate the unity gain frequency for the n channel MOSFET.

Given $C_{gs} = 25fF$, $C_{gd} = 2fF$, $I_D = 100\mu A$ and $\mu Cox\frac{W}{L} = 160\mu A/V^2$. **(05 Marks)**

d. Draw the large signal Eber Moll model for BJT. **(05 Marks)**

6 a. Draw the circuit diagram of a CMOS LNA and explain its operation. **(06 Marks)**

b. Define stern stability factor of an LNA. Determine the stability condition of a cascade stage which exhibits a high reverse isolation i.e. $S_{12} \cong 0$ and $S_{22} \cong 1$. **(04 Marks)**

c. Explain the working of a voltage controlled oscillator with a neat circuit diagram. **(06 Marks)**

d. Suggest one method to employ tuning in VCOs. **(04 Marks)**

7 a. Draw the circuit diagram of a double balanced active mixer and explain the principle of operation. **(08 Marks)**

b. Differentiate SSB and DSB noise figure with respect to RF receivers and state a relationship among them. **(06 Marks)**

c. Explain Hartley oscillator with grounded drain configuration of single transistor oscillator. **(06 Marks)**

8 a. Explain the operation of a charge pump PLL with a neat block diagram. **(10 Marks)**

b. Classify power amplifier based on operating point and sketch circuit diagram for class A power amplifier. **(05 Marks)**

c. Explain feed forward linearization technique employed in power amplifiers with a conceptual diagram. **(05 Marks)**

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